Code No: **20EC3T03** **R20**

II B. TECH I SEMESTER REGULAR EXAMINATIONS, MARCH - 2022
DIGITAL CIRCUITS AND LOGIC DESIGN
(ELECTRONICS AND COMMUNICATION ENGINEERING)

Time: 3 Hours **Max. Marks: 70**

Note: Answer **ONE** question from each unit **(5 × 14 = 70 Marks)**

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UNIT-I

1. a) Identify $(524)_{10}$ in the following code: [6M]
   (i) Binary (ii) Hexadecimal (iii) BCD

   b) Summarize Boolean laws and De-Morgan's theorem with suitable examples. [8M]

(OR)

2. a) Calculate the Boolean expression for a two input Ex-OR gate to realize with the only two input NAND gates and draw the circuit. [7M]

   b) A 7 bit Hamming code is received as 1110101.Predict is there any error? If yes, locate the position of the error bit. Parity checks are created by odd parity. [7M]

UNIT-II

3. a) Illustrate the Boolean function $F = A\left(\overline{A}+B\right)\left(\overline{A}+B+\overline{C}\right)$ into max terms and min terms [7M]

   b) Apply the K-map method to reduce following Boolean function with the don't conditions: [7M]
   F(A, B, C, D)=Σ(0, 6, 8, 13, 14); d(A, B, C, D)=Σ(2, 4,10)

(OR)

4. a) Modify the expression $F = \left(B+BC\right)\left(B+\overline{B}C\right)\left(B+D\right)$ into minimum literals. [7M]

   b) Apply the tabular method to reduce following Boolean function F=Σm(0,2,4,6,7,8,10,12,13,15)+d(1,9,14). [7M]

UNIT-III

5. a) Design a BCD adder using 4-bit parallel binary adder and logic gates. [7M]

   b) Realize a 3 to 8 decoder using 2 to 4 decoder and other required gates. [7M]

(OR)
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6. a) Demonstrate the 4 : 2 priority encoder with a neat logic diagram. [7M]

   b) Implement the following Boolean functions using PLA. [7M]
   $A(x,y,z)= \sum m(0,1,2,4,6)$
   $B(x,y,z)= \sum m(0,2,6,7)$
   $C(x,y,z)=\sum m(3,6)$

UNIT-IV

7. a) Describe the drawback of JK flip-flop? Discuss how it is eliminated in Master Slave flip-flop? [7M]

   b) Build MOD 6 Ripple counter using JK flip-flop and explain the operation. [7M]

(OR)

8. a) Outline the working of flip-flop? How it can be used in sequential circuit and explain in detail. [7M]

   b) Build the circuit diagram of Johnson counter using D-flip-flops and explain its operation with the help of bit pattern. [7M]

UNIT-V

9. a) Demonstrate the logic diagram of Mealy and Moore models and also explain their operation with examples. [7M]

   b) Reduce the following state table to minimum number of states and then draw the state diagram. [7M]

PS	**NS,Z**	
	X=0	**X=1**
A	F,0	B,0
B	D,0	C,0
C	F,0	E,0
D	G,1	A,0
E	D,0	C,0
F	F,1	B,1
G	G,0	H,1
H	G,1	A,0

(OR)

10. a) Discuss the capabilities and limitations of finite state machines? [4M]

    b) Draw the state diagram of a sequence detector which can detect 101 using Melay and Moore models. [10M]

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